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## BIB DATA SHEET

CONFIRMATION NO. 4272

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/588,984	11/21/2006	361	2836	14603-026US1 P2004,0133 U

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## \*\* CONTINUING DATA \*\*\*\*\*

This application is a 371 of PCT/EP05/01476 02/14/2005

## \*\* FOREIGN APPLICATIONS \*\*\*\*\*

GERMANY 10 2004 007 241.8 02/13/2004  
 GERMANY 10 2004 056 222.9 11/22/2004

## \*\* IF REQUIRED, FOREIGN FILING LICENSE GRANTED \*\*

08/08/2008

Foreign Priority claimed	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
35 USC 119(a-d) conditions met	<input checked="" type="checkbox"/> Yes <input type="checkbox"/> No				
Verified and /DHARTI HARIDAS PATEL/ Acknowledged Examiner's Signature	<input type="checkbox"/> Met after Allowance Initials	GERMANY	4	21	2

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 UNITED STATES

## TITLE

Circuit Arrangement and Method For Protecting an Integrated Semiconductor Circuit

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